REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-22 are pending in this application.[1] Claims 1 and 12 are herein amended.

SUPPORT FOR CLAIM AMENDMENTS

Each of independent claims 1 and 12 now consistently recites the first semiconductor layer as a "first conductivity type". That feature is clear from the original specification, see for example Figure 2 and portions in the specification in which the elements 2 and 3 throughout the specification are noted as N type.

Independent claims 1 and 12 also recite "a gate forming region", "at least every first gate being formed in a first gate region", and "the integral semi-insulating plasma CVD nitride film" not extending above an upper portion of "the gate forming region in which said at least every first gate is formed". That subject matter is clear from the original specification, see for example Figure 2 showing a plurality of gates 8 in a region and the CVD nitride film 14 not extending above any of those gates 8 in the region in which they are formed.

ARGUMENTS

(1) Figures 2 and 7-12 were objected to. (2) The specification was objected to for an informality. (3) Claims 1-22 were rejected under 35 U.S.C. § 112, second paragraph. (4) Claims 1-4, 7-9, 12-15, and 18-20 were rejected under 35 U.S.C. § 102(b) as anticipated by applicants' admitted art. (5) Claims 5, 6, 10, 11, 16, 17, 21, and 22 were rejected under 35

[1] The present response amends the claims and in the Listing of Claims section shows the amended claims relative to the original U.S. patent 5,945,692. An Appendix is also submitted showing the claim amendments relative to the previously pending claims, as submitted in the Amendment filed August 29, 2008.

U.S.C. § 103(a) as unpatentable over the admitted art. Those objections and rejections are traversed by the present response as now discussed.

(1) Drawing Objections

Addressing first the objection to the drawings, applicants submit the drawings are proper as the specification does not indicate the gate insulating film 7 and silicon oxide film 161 having a same thickness.

Further, applicants first note the structure in Figure 8 showing the silicon oxide film 161 thicker than a gate insulating film 7 is the same structure as in the background art of Figure 20. Applicants submit although the silicon oxide film 161 is formed on a base layer, as it is not a gate insulating film, the thickness of the silicon oxide film 161 can be larger than the gate insulating film 7 to reduce parasitic capacity. Such an aspect is not essential to the claimed features, and as noted above the background art of Figure 20 has the same configuration.

Applicants further note between the Fig. 7 state and Fig. 8 state, a silicon oxide film is formed, followed by the Fig. 7 state, and a thinner silicon oxide film than a silicon oxide film 16 is formed among patterns of the silicon oxide film 16 used as a mask in forming each impurity layer.

After that, a photoresist is formed to cover the base layer 5 and a guard ring 11 in a peripheral portion, in which a silicon oxide film 161 is formed, and the silicon oxide film in the vicinity thereof. Then, a thin silicon oxide film and the silicon oxide film 16, which is not covered with the photoresist, are eliminated by etching. The original Specification describes this step as: "The oxide film 16 is then etched, if necessary, after photolithography process, ..." in the explanation of Fig. 8. (Specification at col. 11, lines 26-27 et seq).

After the photoresist is eliminated, a silicon oxide film, which becomes the gate insulating film 7, is formed by thermal oxidation. The original Specification describes this step as "...the gate insulating film 7 of silicon oxide is formed by thermal oxidation" in the explanation of Fig. 8. (Specification at col. 11, lines 27-28).

Through this thermal oxidation step, the gate insulating film 7 is formed and a thinner silicon oxide film than the silicon oxide film 16 gets thicker to be the silicon oxide film 161.

At this time, the same phenomenon occurs in a thin silicon oxide film on the guard ring 11 in the peripheral portion, thereby having the same thickness as the silicon oxide film 161. The thickness of the silicon oxide film 16 in the peripheral portion increases as well.

As a result, a configuration as shown in Fig. 8 is obtained. Fig. 8 thereby shows the above-mentioned relationship regarding the thickness of each silicon oxide film would be satisfied.

Thereby, applicants submit it is proper and clear to show the silicon oxide film 161 formed to have a larger thickness than the gate insulating film 7 in Fig. 8.

(2) Specification Objection

Addressing now the objection to the specification, the specification is herein amended to correct the grammatical term noted in the Office Action.

(3) Rejection Under 35 U.S.C. § 112

Addressing now the rejection of claims 1-22 under 35 U.S.C. § 112, second paragraph, that rejection is traversed by the present response as now discussed.

As noted above the claims herein now clarify and consistently refer to the first semiconductor layer as of "first conductivity type". Applicants submit the claims are definite to one of ordinary skill in the art in the formation of the first semiconductor region of a first

conductivity type being selectively formed in the first major surface of the first semiconductor layer.

The outstanding rejection appears to take the position that the first semiconductor layer itself does not "remain" after the selective formation of the first semiconductor region. Applicants submit the claims are definite in that respect. Specifically, and with reference to Figures 2 and 3 in the present specification as a non-limiting example, in the claimed semiconductor device a first semiconductor layer 3 is formed, and then a first semiconductor region of a second conductivity type 11 is selectively formed in that first semiconductor layer 3. The formation of that second conductivity type first semiconductor region 11 results in the first semiconductor layer 3 of the first conductivity type no longer being present where the regions 11 are selectively formed, and thus at portions other than where that first semiconductor region of the second conductivity type 11 is formed the first semiconductor layer 3 will remain. Applicants submit such terminology is clear from the specification and Figures 2 and 3, and applicants submit such terminology is clearly understood by one of ordinary skill in the art.

Applicants respectfully submit the claims also clearly set forth the position and compositional relationship between the first semiconductor region, which is of a second conductivity type, and the first semiconductor layer, which is of a first conductivity type, and that language has been further clarified as noted above.

Applicants respectfully submit the claims are also clear that the first conductivity type first semiconductor layer that remains after the selective formation of the first semiconductor region of the second conductivity type is the element that forms the insular region.

In view of the foregoing comments, applicants respectfully submit each of claims 1-22 is proper under 35 U.S.C. § 112, second paragraph.

(4)-(5) Prior Art Rejections

Addressing now the above-noted prior art rejections over the admitted art, applicants respectfully submit the claims as currently written overcome that rejection.

Each of independent claims 1 and 12 as noted above is amended by the present response to clarify the CVD nitride film does not extend above "an upper portion of the gate forming region in which said at least every first gate is formed". The claims now clarify the structure in the claimed invention that the CVD nitride film does not extend above an upper portion of any first gate in the claimed device, i.e. does not extend above an upper portion of any of the first gates 8. The claim amendments now clarify subject matter indicated in the previous Office Action as not clearly set forth in the claims.[2]

The outstanding Office Action interpreted the admitted art to meet the previously recited claim limitations as in Figure 20 the layer 14 does not extend above the gate 8 underneath the reference indicator 13. However, that gate 8 underneath the reference indicator 13 is only one gate. As clearly shown in Figure 20 in the present specification the CVD nitride film 14 extends above several of the gates 8 in a region of the gates.

Applicants respectfully submit the admitted art does not disclose or suggest the claimed features that an integral semi-insulating plasma CVD nitride film does not extend above an upper portion of a region of at least every of first gates. With reference to Figure 2 in the present specification as a non-limiting example, the semi-insulating plasma CVD film 14 as in the claimed invention does not extend above an upper portion of any of the first gates 8.

Further, the applicants of the present invention recognized in the background art such as shown for example in Figures 19 and 20 in the present specification that a structure is known in which a protective film 14 would extend above different gates 8. The applicants of

[2] Office Action of October 21, 2008, the paragraph bridging pages 9 and 10.

the present invention recognized drawbacks for such a system, discussed throughout the "Description of the Background Art" section of the present application.

The applicants of the present invention in recognizing problems in the background art also recognized a solution to the problems, and particularly the solution being in limiting the extent of the CVD nitride film to not extend above an upper portion of a region in which all of first gates are formed. Without recognizing the problems in the background art pointed out in the specification, one of ordinary skill in the art would clearly not have been led to any solution of such problems, and particularly would not have been led to a solution that limits the extent of the CVD nitride film such as in the claims as written.

Moreover, the outstanding grounds for rejection is ignoring the fact that the admitted art does not even recognize any problems therein or any solution to such problems. The claimed invention recognized drawbacks in the admitted art and a specific solution of limiting the extent of a CVD nitride film to not extend above an upper portion of a region of all of first gates to solve such problems. Applicants submit such a structure is not disclosed in the admitted art and the admitted art does not achieve the benefits realized by the claimed structure.

Thereby, each of independent claims 1 and 12 as currently written is believed to positively recite a structure neither taught nor suggested by the admitted art of Figure 20. Thereby, each of claims 1-22 is believed to be allowable over the noted admitted art.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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APPENDIX

Listing of Claims

1. (Currently Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type having first and second major surfaces;

a first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first conductivity type first semiconductor layer remains along a peripheral portion of said first major surface, and said first conductivity type first semiconductor layer remains in a form of an insular region in a planar view in a central portion of said first major surface;

a second semiconductor region of the first conductivity type formed in a surface of said first semiconductor region, with a channel region provided between said second semiconductor region and said insular region of said first semiconductor layer;

a gate insulating film formed on a surface of said channel region;

a ~~first~~ gate forming region formed on said gate insulating film, at least every first gate being formed in a first gate region;

an interlayer insulating film formed at least on said first gate:

a first main electrode formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being electrically connected to said second semiconductor region and having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of said first semiconductor layer; and

an integral semi-insulating plasma CVD nitride film covering at least the peripheral portion of said first major surface other than the central portion of said first major surface and not extending above an upper portion of [[a]] the gate forming region in which said at least every first gate is formed, said integral semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.

2. (Original) The semiconductor device of claim 1, wherein

said plasma CVD nitride film extends from the peripheral portion of said first major surface to a surface of said first main electrode at said end.

3. (Previously Presented) The semiconductor device of claim 1, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected.

4. (Original) The semiconductor device of claim 3, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

5. (Original) The semiconductor device of claim 4, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

6. (Original) The semiconductor device of claim 4, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

7. (Original) The semiconductor device of claim 1, further comprising:

a second semiconductor layer of the second conductivity type formed between said second major surface of said first semiconductor layer and said second main electrode.

8. (Previously Presented) The semiconductor device of claim 7, further comprising:
a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate electrode and said second gate electrode are integrally formed and electrically connected.

9. (Previously Presented) The semiconductor device of claim 8, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

10. (Original) The semiconductor device of claim 9, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

11. (Original) The semiconductor device of claim 9, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

12. (Currently Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type having first and second major surfaces;

at least one first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first conductivity type first semiconductor remains along a peripheral portion of said first major surface, and said first conductivity type first semiconductor region remains in a form of a plurality of insular regions in a planar view in a central portion of said first major surface;

a plurality of second semiconductor regions of the first conductivity type formed in a surface of said at least one first semiconductor region, with channel regions provided between said second semiconductor regions and said insular regions of said first semiconductor layer;

a gate insulating film formed on a surface of said channel regions;

a ~~first~~ gate forming region formed on said gate insulating film, at least every first gate being formed in a first gate region;

an interlayer insulating film formed at least on said first gate:

a first main electrode formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being

electrically connected to said plurality of second semiconductor regions, said first main electrode further having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of said first semiconductor layer; and

an integral semi-insulating plasma CVD nitride film for covering at least the peripheral portion of said first major surface other than the central portion of said first major surface and not extending above an upper portion of [[a]] the gate forming region in which said at least every first gate is formed, said integral semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.

13. (Original) The semiconductor device of claim 12, wherein

said plasma CVD nitride film extends from the peripheral portion of said first major surface to a surface of said first main electrode at said end.

14. (Previously Presented) The semiconductor device of claim 13, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected.

15. (Original) The semiconductor device of claim 14, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

16. (Original) The semiconductor device of claim 15, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

17. (Original) The semiconductor device of claim 15, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

18. (Original) The semiconductor device of claim 13, further comprising:

a second semiconductor layer of the second conductivity type formed between said second major surface of said first semiconductor layer and said second main electrode.

19. (Previously Presented) The semiconductor device of claim 18, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected.

20. (Original) The semiconductor device of claim 19, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

21. (Original) The semiconductor device of claim 20, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

22. (Original) The semiconductor device of claim 20, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).